

Digital System Design and Implementation in ASIC and FPGA

The lecture topics and laboratory assignments will be structured in such a manner that the incoming undergraduate student will not be expected to have a detailed background in digital design. Basic topics in digital design, circuit design, and VHDL will be covered in detail. The *FPGA and Digital Electronics Research Lab* (CS 301) will be used to conduct lectures and laboratory experiments.

At the end of 8 weeks participants in the program would have gained the following skills:

- Digital Logic and Circuit Design
- Digital Design using VHDL
- Design Implementation in ASIC and FPGA
- Digital Design using Electronic design automation (EDA) tools

The \$1000 provided to the students is planned to be used for the FPGA board and textbook purchases which students will retain at the end of the program. This gives them the opportunity to practice the acquired skills on their individual board using examples in the textbook.

The following is the proposed schedule of topics to be covered in the 8 week program:

Week 1: Basic Digital Electronics and Logic Design

Topics covered: Introduction to characteristics and elementary applications of field-effect transistors, binary, octal, decimal, hexadecimal-number base conversions, complements, signed binary numbers, binary arithmetic, de-morgan's theorem, principle of duality, boolean expression, boolean function, minimization of boolean expressions, sum of products (SOP), product of sums (POS), minterm, maxterm, canonical forms, conversion between canonical forms, karnaugh map minimization.

Software used: MultiSim 10.1

Week 2 - 3: Combinational and Sequential Circuit Design

Topics covered: Logic Gates: AND, OR, NOT, NAND, NOR, exclusive-OR and exclusive-NOR, implementations of logic functions using gates, NAND - NOR implementations, multi level gate implementations, Multi output gate implementations. Combinational Circuits: design procedure, adders, subtractors, serial adder / subtractor, parallel adder / subtractor, carry look ahead adder, BCD adder, magnitude comparator, multiplexer/ demultiplexer, encoder / decoder. Sequential Circuits: Flip flops SR, JK, T, D and Master slave, characteristic table and equation, edge triggering, level triggering, asynchronous and synchronous counters, modulo, classification of sequential circuits, moore and mealy, design of synchronous counters: state diagram, state table, state minimization, state assignment, register, shift registers, universal shift register, shift counters, ring counters.

Software tools used: MultiSim 10.1

Week 4 - 5: Digital design with VHDL

Topics covered: Introduction to various modeling methods, timings, events, propagation delays and concurrency, the language constructs, data representations and formats, and physical attributes.

Software tools: MultiSim 10.1, ModelSim SE

Week 6: Introduction to ASIC and FPGA design

Topics covered: Introduction to digital design in application-specific integrated circuit (ASIC) and field-programmable gate array (FPGA), FPGA fabrics, combinational and sequential logic design using hardware description languages (HDL), register transfer and behavioral design, automated design synthesis using Electronic design automation (EDA) tools. Schematic capture and functional simulation, post-place and route simulation and implementation on FPGA.

Software tools: Mentor Graphics Custom Design, ModelSim SE, Xilinx ISE

Hardware board: Spartan 3-200K system boards (S3BOARD, Xilinx Spartan-3 FPGA w/ twelve 18-bit multipliers, 216Kbits of block RAM, running at 200 MHz internal clock speeds).

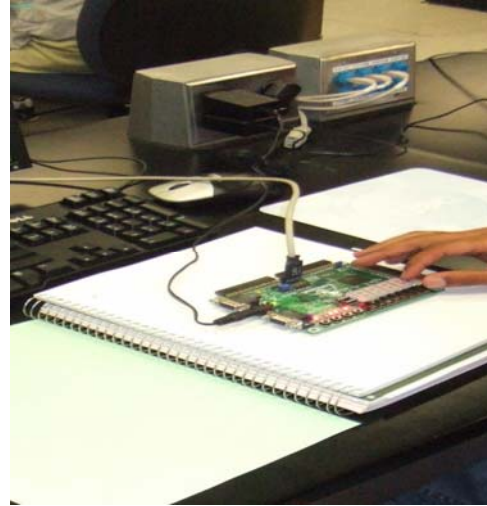
Week 7 - 8: FPGA implementation and verification of the Data Collector module in the Ultrasound Array Transducer chip

Topics covered: Data collector module will be written in VHDL, conduct schematic capture and functional simulation, perform post-place and route simulation and implementation on FPGA.

Software tools: Mentor Graphics Custom Design, ModelSim SE, Xilinx ISE

Hardware board: Spartan 3-200K system boards (S3BOARD, Xilinx Spartan-3 FPGA w/ twelve 18-bit multipliers, 216Kbits of block RAM, running at 200 MHz internal clock speeds).

FPGA and Digital Electronics Research Lab



The facilities in this laboratory support undergraduate and graduate courses in use of digital logic circuit design and, programmable logic circuits (FPGA) design. The lab is equipped with 21 stations with Pentium 4/ Pentium D processors, 1 projector, 2 printers, National Instruments DAQ, PCI-GPIB cards, and 25 Spartan 3-200K system boards (S3BOARD, Xilinx Spartan-3 FPGA w/ twelve 18-bit multipliers, 216Kbits of block RAM, running at 200 MHz internal clock speeds).

We have a wide range of tools available for student use including:

- Leonardo Spectrum
- MultiSim 10.1
- ModelSim SE
- Xilinx ISE
- Freescale CodeWarrior
- LabView 8.2
- Quartus II 7.0
- Matlab 7.5
- MicroWind
- PSpice 10.5